

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* SUDIPTO RANENDRA ROY

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Appeal No. 2001-2388  
Application 09/151,948

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ON BRIEF

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Before OWENS, WALTZ and KRATZ, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

*DECISION ON APPEAL*

This is an appeal from the final rejection of claims 1-27, which are all of the claims in the application.

*THE INVENTION*

The appellant claims a method for making a liquid crystal display integrated circuit device. Claim 1 is illustrative:

1. A method of fabricating a liquid crystal display integrated circuit device comprising:

providing semiconductor device structures in and on a semiconductor substrate wherein said semiconductor device structures are covered by an insulating layer;

patterning a trench into said insulating layer and a via opening within said trench through said insulating layer to one of said underlying semiconductor device structures;

depositing a metal layer overlying said insulating layer and within said trench and said via opening;

polishing away said metal layer overlying said insulating layer leaving said metal layer within said trench to form a metal pixel and within said via opening to form an interconnect between said metal pixel and said underlying semiconductor device wherein the top surface of said substrate is planarized;

depositing a passivation layer overlying said top surface of said substrate;

forming a liquid crystal material layer overlying said passivation layer and;

attaching a second semiconductor substrate overlying said liquid crystal material layer to complete the fabrication of said liquid crystal display integrated circuit device.

*THE REFERENCES*

Huang et al. (Huang)	5,635,423	Jun. 3, 1997
Jeong	5,960,317	Sep. 28, 1999
		(filed Sep. 26, 1997)

*THE REJECTIONS*

The claims stand rejected as follows: claims 1-4, 6-15 and 17-21 over the appellant's admitted prior art in view of Huang, and claims 5, 16 and 22-27 over the appellant's admitted prior art in view of Huang and Jeong.

*OPINION*

We reverse the aforementioned rejections. We need to address only claim 1, which is the broadest independent claim.

The appellant acknowledges (specification, page 2) that it was known in the art to 1) form on a semiconductor substrate (10) in the following order, as shown in figure 1, a barrier/glue layer (20), first metal lines (22), an optional anti-reflective coating (24), and an insulating layer (26), 2) form patterned openings in the insulating layer, 3) fill the openings with tungsten to form tungsten plugs (28), and 4) form over the tungsten plugs, in the following sequence, a second barrier layer (30), metal pixels (32), an undoped silicate glass (34)/silicon nitride (36) passivation layer, a liquid crystal layer (52), and a top substrate (56).

In the "description of the prior art" section of the specification (pages 2-3) the appellant points out that the thickness of the liquid crystal layer in figure 1 is less at

point A than at point B, and states that "[f]or sharp display, high speed, and good performance, it is critical that the liquid crystal maintain a constant gap between the top and bottom substrates."<sup>1</sup>

The appellant obtains this constant gap by use of the dual damascene technique in which a trench (29) and a via opening (27) are formed in an insulating layer (26), a metal layer (40) is formed over and within the trench and the via opening (figure 4), and the metal layer above the surface of the insulating layer is polished away to form a planarized surface having below it a metal-filled trench (44), i.e., a metal pixel, and a metal-filled via opening (42) that connects the metal pixel to an underlying semiconductor device (14, 16) (figure 5). A passivation layer (34 and 36), a liquid crystal layer (52) and a top substrate (56) are formed over the planarized surface. As shown in figure 6, the thickness of the liquid crystal layer is the same above and between the metal pixels.

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<sup>1</sup> The examiner has not established that the disclosed criticality of the constant gap pertains to the acknowledged prior art rather than being a discovery by the appellant.

Huang teaches that when conductive lines are formed by the traditional method of etching a metal layer, it is extremely difficult to form a planarized layer after filling in the spaces between the conductive lines, and there are other difficulties such as void formation between the conductive lines, trapping of impurities and volatile materials in the spaces between conductive lines, and "poor metal step coverage, residual metal shorts leading to inconsistent manufacturability, low yields, uncertain reliability and poor ultra large scale integration extendability" (col. 1, lines 35-53).

Huang's method is a dual damascene technique wherein trenches and vias are simultaneously filled with conductive material (col. 5, lines 30-33). The method forms an interconnection structure comprising conductive lines and conductive vias wherein the distance between conductive lines preferably is less than about 0.35 micron, thereby improving the density and ultra large scale integration (col. 5, lines 17-27; col. 9, lines 38-56).

The examiner argues that it would have been obvious to one of ordinary skill in the art to use Huang's method instead of the admitted prior art method to form an interconnect/metal pixel structure "since the method of Huang used to produce an

interconnect/metal pixel structure would result in improved interconnect/metal pixel structure density and ultra large-scale integration over the interconnect/metal pixel structure of the admitted prior art" (answer, pages 4-5). The examiner, however, has not established that the benefit of Huang's method, i.e., formation of planarized layers having a wiring line spacing of preferably less than about 0.35 micron, would have been desired by one of ordinary skill in the art when forming the admitted prior art structure having an unplanarized passivation layer on metal pixels. For a *prima facie* case of obviousness to be established, the teachings from the prior art itself must appear to have suggested the claimed subject matter to one of ordinary skill in the art, see *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976), and the examiner has not established that the applied prior art itself would have provided one of ordinary skill in the art with a suggestion to use Huang's method to form an interconnect/metal pixel structure.

The examiner argues that "*Huang et al.* taught an alternate, dual damascene, method of forming a structure equivalent to the interconnect/metal pixel structure described in the appellants' [sic, appellant's] admitted prior art" (answer, page 11). This argument is not persuasive because the examiner has not provided

evidence or technical reasoning which shows that Huang's structure and that of the appellant's admitted prior art are equivalent.

The examiner argues that it would have been obvious to one of ordinary skill in the art to use Huang's dual damascene method instead of the appellant's admitted prior art method for making a liquid crystal display integrated circuit device because Huang teaches that an etch back method (which appears to be the method used to form the metal pixels in the appellant's admitted prior art structure) has the disadvantage of residual metal shorts leading to inconsistent manufacturability, low yields, uncertain reliability, and poor ultra large scale extendability (answer, pages 10-11). Huang's disclosed disadvantage of an etch back method relied upon by the examiner, and the additional disclosed disadvantages set forth above in the discussion of Huang, are in the context of ultra large scale integration semiconductor wiring having planarized layers with minimum spacing between wiring lines (col. 1, lines 17-20). The examiner has not established that one of ordinary skill in the art would have considered these disadvantages to exist in the appellant's admitted prior art liquid crystal display integrated circuit device having metal pixels instead of minimum-spaced conductive wiring and having on

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the metal pixels an unplanarized passivation layer.

For the above reasons, we conclude that the examiner has not carried the burden of establishing a *prima facie* case of obviousness of the appellant's claimed invention.<sup>2</sup>

*DECISION*

The rejections of claims 1-4, 6-15 and 17-21 over the appellant's admitted prior art in view of Huang, and claims 5, 16 and 22-27 over the appellant's admitted prior art in view of Huang and Jeong, are reversed.

*REVERSED*

	)	
TERRY J. OWENS	)	
Administrative Patent Judge	)	
	)	
	)	
	)	BOARD OF PATENT
THOMAS A. WALTZ	)	
Administrative Patent Judge	)	APPEALS AND
	)	
	)	INTERFERENCES
	)	
PETER F. KRATZ	)	
Administrative Patent Judge	)	

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<sup>2</sup> The examiner does not rely upon Jeong for any teaching which remedies the above-discussed deficiency in the appellant's admitted prior art and Huang.



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